CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for accessing data comprising the acts of:

receiving a request to read a block of consecutive words from an array of synchronous random access memory;

addressing the array;

initiating a first read burst from the array;

iterating a transfer, the transfer comprising the acts of:

reading a word of error-free data from the array, the word of data containing error detection redundancy bits;

confirming an absence of errors in the word of error-free data by performing an error detection algorithm upon the word;

and

placing a copy of the word of error-free data into a FIFO;

reading a further word of data from the array;

detecting a correctable error in the further word of data;

terminating the first read burst;

correcting the further word to form a corrected word;

placing a first copy of the corrected word into the FIFO;

writing a further copy of the corrected word into the array;

initiating a second read burst from the array; and

further iterating the transfer, whereby the request is honored.

2. The method of claim 1 wherein the correctable error is a single bit error.

3. The method of claim 1 wherein the terminating is performed in response to the detecting.

4. The method of claim 1 wherein the terminating is performed after the detecting and prior to any further reading.

5. A memory storage device controller comprising:

a Read FIFO;

a Write FIFO;

a Writeback FIFO;

a bidirectional port connected to a synchronous RAM array, the synchronous RAM array operable to respond to commands;

a multiplexer operable to supply data to the port;

a command processor having an input operable to receive data from the Write FIFO, the command processor further operable to supply formatted RAM commands to the multiplexer;

an encoder having an input operable to receive data from the Write FIFO and to supply encoded data to the multiplexer;

an EDC (error detection and correction) block having an input operable to receive data from the port and further having an output operable to supply data to the Read FIFO and Writeback FIFO, the EDC block, the EDC block operable to correct correctable data errors and to detect uncorrectable data errors; and

an address block controlled by the command processor, the address block operable to supply addresses to the multiplexer.

6. The memory storage device controller of claim 5 further comprising:

a direct memory access (DMA) controller operable to supply data to the Write FIFO and to receive data from the Read FIFO.

7. The memory storage device controller of claim 5 wherein:

the encoder and the EDC block are state machines.

8. The memory storage device controller of claim 7 wherein:

the command processor, the encoder, and the EDC block are each part of a respective field programmable gate array.

9. The memory storage device controller of claim 7 wherein the memory storage device controller is in a single field programmable gate array.

10. The memory storage device controller of claim 9 wherein the address block is a table RAM.

11. The memory storage device controller of claim 1 wherein the address block is a table RAM.